AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

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1. (Currently Amended) A computing system comprising:

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a processor with various power state conditions, wherein the processor performs at a selectable operating mode;

a north-bridge controller initiating a processor reset signal input;

a south-bridge controller providing an interface for I/O devices to the processor and performing power state transitions from the I/O devices to the south-bridge controller;

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a clock;

a power supply; and

a logic device interfaced to the processor, the north-bridge ~~controller;~~controller, the south-bridge ~~controller;~~controller, the ~~clock;~~clock, and the power supply, whereby the logic device asserts a transition to a different operating mode on the processor while the processor is in a deep sleep power state, and upon transition back to operating power state, the clock provides a frequency and the power supply provides a voltage matched to the different operating mode.

2. (Original) The computing system of claim 1 wherein the logic device monitors a reset condition of the processor, waits for reset to be de-asserted and asserts a performance mode transition.

3. (Original) The computing system of claim 1 wherein the logic device passes transition signals from the north-bridge controller to the processor, the transition

signals placing the processor in a deep sleep power state and asserting a performance mode transition.

4. (Currently Amended) The computing system of claim 1 wherein the logic device passes transition signals from the ~~north-bridge~~ south-bridge controller to the processor, the transition signals placing the processor in a deep sleep power state and asserting a performance mode transition.

5. (Original) The computing system of claim 1 wherein the logic device asserts the transition during the normal processor power up sequence.

6. (Original) The computing system of claim 1 wherein the logic device asserts the transition following the processor first read only memory (ROM) access.

7. (Cancelled).

8. (Cancelled).

9. (Cancelled).

10. (Cancelled).

11. (Currently Amended) A method of transitioning a processor having various power state conditions wherein the processor operates a selectable operating mode, ~~the method~~ comprising:

providing a north-bridge controller, the north-bridge controller initiating a processor reset signal input;

passing control signals from ~~a~~ the north-bridge controller capable of placing the processor in a deep sleep state and transitioning the processor into a different operating ~~mode.~~mode;

providing a south-bridge controller, the south-bridge controller providing interface for I/O devices to the processor and performing power state transitions from the I/O devices to the south-bridge controller;

passing control signals from the south-bridge controller capable of placing the processor in a deep sleep state and transitioning the processor into a different operating mode;

waiting for the processor to reach a reset state;

resetting the processor; and

asserting a performance mode change in the processor.

12. (Cancelled).

13. (Cancelled).

14. (Currently Amended) The method of claim ~~13~~ 11 wherein asserting a performance mode is during normal processor power up sequence.

15. (Currently Amended) The method of claim ~~13~~ 11 wherein asserting a performance mode is during processor read only memory (ROM) access.